## REMARKS

Claims 1, 3, 9, 30-32, 34, 35, 37, and 40, 42, and 44 are rejected as being anticipated under 35 U.S.C. 102(e) by Rhee, *et al.* (United States Patent Number 6,774,712). Claims 39, 41 and 43 are deemed to be inherent since, according to the Office Action at page 4, fourth paragraph, the claimed structure is anticipated by Rhee, *et al.* Applicants therefore assume that claims 39, 41 and 43 are likewise rejected under 35 U.S.C. 102(e) by Rhee, *et al.* Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Sher (United States Patent Number 6,633,196). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Bae, *et al.* (United States Patent Number 6,373,754). Claims 33, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Park, *et al.* (United States Patent Number 5,349,559). Claims 10-12, 14-17, 23, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (United States Publication Number 2002/0053943) in view of Sher. In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections is respectfully requested.

Independent claims 1, 10, 23, and 34 are amended herein to clarify that a semiconductor device comprises a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits.

Independent claims 35 and 37 are amended herein to clarify that a an internal voltage

generating circuit of a semiconductor device comprises a control signal generating circuit that generates a control signal according to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device.

The features of the present invention as claimed in amended independent claims 1, 10, 23, 34, 35, and 37 are illustrated at least at Figure 2 and corresponding text of the specification as filed. As shown in Figure 2, a control signal generating circuit 20 generates a control signal C that is responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device (see Figure 2 and page 9, paragraph [0030] of the specification as filed). The control signal C is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits (for example, 38 bits), and the control signal C is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits (for example, 18 bits) (see page 7, line 23 through page 8, line 4 of the specification as filed).

The semiconductor device of the present invention as claimed in independent claims 1, 10, 23, 34, 35, and 37 can be further explained by distinguishing the present invention from a conventional semiconductor device illustrated in the Background of the Invention section of the specification as filed. As shown in Figure 1 of the Background of the Invention section of the present specification, a conventional semiconductor device includes an internal voltage generating circuit for a memory cell array, a peripheral circuit, and a delay locked loop, the internal voltage generating circuit including a comparator 10 and a driver D (see Figure 1 of the present specification). The conventional internal voltage generating circuit shown in Figure 1 generates a constant internal voltage IVC <u>independently from</u> a data input/output bit number that is received and output by the conventional semiconductor device, for example, data (bits) of bit line pairs of a memory cell array (see pages 2-3, paragraph [0008] of the specification as filed). In other words, in the conventional semiconductor device, the internal voltage IVC is in no way generated in response to the number of data bits processed by the conventional semiconductor

device. As a result, in the conventional semiconductor device, when a data input/output bit number is increased, a level drop of the internal voltage for a memory cell array does not occur, but a level drop of the internal voltage for a peripheral circuit or a delay locked loop can occur, causing data access speed to be degraded (see page 3, lines 2-5, 16-20 of the specification as filed).

The present invention, in contrast to the abovementioned conventional semiconductor device, includes an internal voltage generating circuit that receives a control signal C from a control signal generating circuit 20, wherein the state of the control signal is changed, i.e., either a "high" level or a "low level," according to the number of bits being input to the device or output from the device, to set the internal voltage IVC to a reference voltage VREF or an external voltage EVC level, respectively (see, for example, Figure 2 and see page 9, paragraph [0030] of the specification as filed). In this manner, in contrast to the conventional semiconductor device, data access speed is improved in the present invention despite an increase in a data input/output bit number (see page 4, paragraph [0012], and page 14, paragraph [0050] of the specification as filed).

With regard to the rejections of independent claims 1 and 34 based on Rhee, *et al.,* it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 34.

Examiner continues to maintain that the control signal PDPDEB of Rhee, *et al.* is

analogous to a control signal, as claimed in claims 1 and 34. Specifically, the current Office Action at page 2 refers to control signal PDPDEB of Rhee, *et al.* being a control signal generated responsive to an input signal related to a number of bits being processed by the semiconductor device of Rhee, *et al.* However, there is no teaching or suggestion in Rhee, *et al.* of control signal PDPDEB of Rhee, *et al.* being a control signal generated responsive to an input signal related to a number of bits being simultaneously input to the semiconductor device or output from by the semiconductor device of Rhee, *et al.* Instead, control signal PDPDEB of Rhee, *et al.,* as well as control signal PDPDE of Rhee, *et al.,* are determined by a control command that is input from outside the chip, or by a transition of a voltage level at a specific pin of the chip (see Rhee, column 3, lines 18-20).

The Office Action at page 11 states that "a change from a low to high or a high to low can be considered a bit." Applicants assume that Examiner is referring to a transition of a voltage level, for example, either a voltage level applied to a gate of a transistor, or the abovementioned transition of a voltage level at a specific pin of the chip. Even if a low to high transition or high to low transition of a voltage level is arguably considered a bit, there is no teaching or suggestion in Rhee, *et al.* of the voltage level being a control signal responsive to an input signal that is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34.

The Office Action at page 11 further refers to a control signal being inherent in a transistor because a transistor acts as a switch and must be controlled at the input of the gate or base. Applicants agree that a fundamental feature of a transistor is that a transistor can act as a switch by applying a voltage to a gate or base of a transistor. However, this statement is irrelevant with regard to comparing the present invention as claimed to Rhee, *et al.*, since, as previously stated, there is no teaching or suggestion in Rhee, *et al.* of a control signal at the input of the gate or base of the transistor being responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34. Nor is there any

teaching or suggestion that the control signal at the input of the gate or base of the transistor being activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, or being inactivated when the input signal indicates that the number of data bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 34. Examiner provides no explanation in the Office Action of a control signal being applied to the gate of the hypothetical transistor described in the Office Action being responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34.

The Office Action at page 11 further attempts to draw an analogy between the present invention as claimed in claims 1 and 34 and Rhee, *et al.* by asserting that a change in voltage is considered to be a "bit" that is applied to a gate of a transistor, wherein the "bit" is compared to a threshold voltage of the transistor. However, if this reasoning is to be accurate, then, in order for the threshold voltage to be analogous to a single bit of a predetermined number of bits, according to Examiner's definition of a "bit," the threshold voltage would also need to change from high to low or from low to high. However, there is no such teaching or suggestion in Rhee, *et al.* of a transistor having a threshold voltage changing from low to high or high to low.

Moreover, even if the threshold voltage is arguably analogous to a predetermined number of 0 bits, as asserted in the Office Action at page 11, there is no teaching or suggestion in Rhee, *et al.* of the predetermined number of bits being greater than one bit, as claimed in claims 1 and 34. A single transistor, as described in the Office Action, has a single threshold voltage, and does not have a predetermined number of bits being greater than one bit, as claimed in claims 1 and 34.

With regard to the rejections of independent claims 35 and 37 based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for

generating a control signal according to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 35 and 37, for reasons similar to those described above with regard to independent claims 1 and 34.

In addition, with regard to the rejection of independent claim 37 based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claim 37. This difference between the present invention as claimed in claim 37 and Rhee, *et al.* can be explained by way of example. As shown in Figure 3 of the drawings as filed, a comparing circuit includes a comparator 10 that is connected between the external power voltage EVC and a first node and compares a reference voltage VREF to an internal voltage IVC to generate a driving signal, and a switching circuit N2 connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator 10 when C control signal C is activated, as claimed in independent claim 37. There is no such teaching or suggestion in Rhee, *et al.* of this claimed feature. Specifically, there is no teaching or suggestion in Rhee, *et al.* of a switching circuit connected between a first node and a ground voltage and cutting off the ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claim 37.

With regard to the rejection of claim 9, claim 9 is amended herein to clarify that a signal generating circuit comprises a mode setting circuit that sets a mode of the semiconductor device, and generates a control signal in response to an input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits. Accordingly, it is submitted that there is no teaching or suggestion in Rhee, et al. of a signal generating circuit comprising a mode setting circuit that sets a mode of the semiconductor device, and generating a control signal in

response to an input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits, as claimed in amended claim 9. While the Office Action at page 3 refers to an input signal changing modes between a saturation mode, active mode, etc. in a transistor, there is no teaching or suggestion of a mode setting circuit that sets a mode of the semiconductor device, as claimed in claim 9, noting that the semiconductor device as claimed in claim 1 to which claim 9 depends includes a control signal generating circuit and an internal voltage generating circuit. Further, Applicants submit that amended claim 9 is not a statement of intended use, but, rather, is a limitation that recites a structural component of the present invention.

With regard to the rejections of claims 30-32 based on Rhee, *et al.*, claims 30-32 are amended herein to clarify that a mode setting circuit produces a value that is represented by mode setting bits and a mode setting command, wherein a control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by a semiconductor device. It is submitted that Rhee, *et al.* fails to teach or suggest a mode setting circuit that produces a value that is represented by mode setting bits and a mode setting command, wherein a control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by a semiconductor device. With regard to statements made in the Office Action at page 4, Applicants submit that amended claims 30-32 are not statements of intended use, but, rather, are limitations that recite a structural component of the present invention.

For at least the reasons described herein, it is submitted that Rhee, *et al.* fails to teach or suggest the invention set forth in the amended claims. Reconsideration of the rejections of claims 1, 3, 9, 30-32, 34, 35, 37 and 39-44 under 35 U.S.C. 102(e) based on Rhee, *et al.* is respectfully requested.

With regard to the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination Rhee, *et al.* and Sher, and the rejection of claim 2 under 35 U.S.C. 103(a) based on

the combination of Rhee, *et al.* and Bae, *et al.*, and the rejections of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.,* it is submitted that Rhee, *et al.* is disqualified as a prior art reference to the present application, pursuant to 35 U.S.C. 103(c), since Rhee, *et al.* was subject to an obligation of assignment to the same entity as the present application at the time the present invention was made, as affirmed by the following statement:

Statement Concerning Common Ownership

The present United States Patent Application 10/799,783 and United States Patent Application 10/331,602 (now United States Patent No. 6,774,712) were, at the time the invention of the present Application 10/799,783 was made, subject to assignment to Samsung Electronics Co., Ltd.

Accordingly, reconsideration and removal of the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Sher are respectfully requested. In addition, reconsideration and removal of the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Bae, *et al.* are respectfully requested. In addition, reconsideration and removal of the rejections of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.* are respectfully requested.

Further, none of the remaining references (Sher, Bae, *et al.*, Park, *et al.*) support a substitute rejection of any of the claims based on lack of novelty (35 U.S.C. §102) or based on obviousness (35 U.S.C. §103).

With regard to the rejection of claims 10-12, 14-17, 23, 25, and 27-29 based on the combination of Yamasaki, *et al.* and Sher, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or suggests a semiconductor device, comprising a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device,

wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in independent claims 10 and 23. In addition, neither Yamasaki, *et al.* nor Sher teaches or suggests an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23.

The Office Action at pages 14-15 refers to the combination of Yamasaki, *et al.* and Sher as teaching a predetermined number of bits being 0. However, there is no teaching or suggestion in either Yamasaki, *et al.* or Sher of a predetermined number of bits being greater than one bit, as claimed in amended independent claims 10 and 23.

Further, the Office Action at page 6 refers to a test mode setting circuit 3 of Yamasaki (see Yamasaki, Figure 5A) as being a control signal generating circuit. In particular, Yamasaki, *et al.* teaches that the test mode setting circuit 3 generates a test mode designating signal TE, and teaches a driving circuit 2 that is activated in response to the test mode designating signal TE (see Yamasaki, Figures 1 and 5A and page 5, paragraph [0068], lines 6-11). The Office Action further states at page 15, lines 1 and 2 that a voltage down converter VDC of Yamasaki, *et al.* is coupled to the mode setting circuit 3 via a transfer gate 2c. Applicants respectfully disagree with this assertion. Applicants' previous response, entitled Amendment E, filed on May 9, 2007, included the following statements:

> Further, even if the test mode designating signal TE of Yamasaki, *et al.* is a control signal, there is no teaching or suggestion in Yamasaki, *et al.* of an internal voltage generating circuit being coupled to the control signal generating circuit for receiving the control signal, as claimed in independent claim 10. Specifically, there is no teaching or suggestion of voltage down converter VDC of Yamasaki,

> *et al.* being coupled to the test mode setting circuit 3. Moreover, the voltage down converter VDC of Yamasaki, *et al.* does not receive the test mode designating signal TE of Yamasaki, *et al.* Instead, the test mode designating signal TE of Yamasaki, *et al.* is applied to the driving circuit 2 of Yamasaki, *et al.* In addition, as described above, the voltage down converter VDC of Yamasaki, *et al.* is similar to a conventional internal voltage generating circuit, for example, the circuit shown in Figure 1 of the present specification. It therefore follows that the voltage down converter VDC of Yamasaki, *et al.* is different than Applicants' claimed internal voltage generating circuit.

With regard to the statement in the current Office Action regarding the voltage down converter VDC of Yamasaki, *et al.* being coupled to the mode setting circuit 3 via a transfer gate 2c, Applicants point out that transfer gate 2c of Yamasaki, *et al.* is coupled between a differential amplifier 2b and a drive transistor 2d (see Yamasaki, Figure 1), and includes a gate to which the test mode designating signal TE is applied. Contrary to the abovementioned assertion made in the Office Action, there is no teaching or suggestion in Yamasaki, *et al.* of the transfer gate 2c being coupled to the voltage down converter VDC. Therefore, there is no teaching or suggestion in Yamasaki, *et al.* of the voltage down converter VDC being a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 10 and 23.

Further, as shown in Figure 1 of Yamasaki, *et al.*, the driving circuit 2 is connected to an input of the comparator CMP of the voltage down converter VDC. However, in order for the voltage down converter VDC of Yamasaki, *et al* to be analogous to an internal voltage generating circuit, as claimed, then the voltage down converter VDC must be coupled to the driving circuit 2 in a manner that permits the voltage down converter VDC to receive the test mode designating signal TE (referred to in the Office Action as a control signal). Specifically, the test mode designating signal TE must be applied to a switching circuit that is coupled to both the mode setting circuit 3 (referred to in the Office Action as a control signal generating circuit) and an output of a comparing circuit (referred to in the Office Action as comparator CMP). As

shown in Figure 1 of Yamasaki, et al., the test mode designating signal TE is applied only to transfer gates 2c and 2e, and to transistor 2f coupled to differential amplifier 2b. The comparator CMP of the voltage down converter VDC of Yamasaki, *et al.* has two inputs Vref, IVL, and an output coupled to a drive transistor 2d. There is no teaching or suggestion in Yamasaki, *et al.* of the voltage down converter VDC of Yamasaki, *et al.* being an internal voltage generating circuit coupled to a control signal generating circuit for receiving a control signal, as claimed in claims 10 and 23. Although the driving circuit 2 of Yamasaki, *et al.* is coupled to an input (Vref) of the comparator CMP of the voltage down converter VDC, there is no teaching or suggestion of the voltage down converter VDC receiving the test mode designating signal TE.

Sher likewise fails to teach or suggest a semiconductor device, comprising a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in independent claims 10 and 23. In addition, Sher likewise fails to teach or suggest an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23.

Accordingly, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the invention set forth in amended independent claims 10 and 23. Since the combination of Yamasaki, *et al.* and Sher fails to teach or suggest the invention set forth in the claims, the claims are believed to be allowable over the cited

references. Accordingly, reconsideration and removal of the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher are respectfully requested.

In view of the amendments to the claims and the specification, and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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